WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising the steps of:

preparing a semiconductor substrate having a memory cell area and a logic circuit area defined on a principal surface of the semiconductor substrate;

forming a gate insulating film on the principal surface of the semiconductor substrate;

forming a silicon film on the gate insulating film;

doping impurities into the silicon film to make a region of the silicon film in the memory cell area having a first impurity concentration and to make a region of the silicon film in the logic circuit area having a second impurity concentration lower than the first impurity concentration;

patterning the silicon film to leave word lines having the first impurity concentration and serving as gate electrodes in the memory cell area and to leave gate electrodes having the second impurity concentration in the logic circuit area; and

forming source/drain regions of MISFET's in a surface layer of the semiconductor substrate by doping impurities into regions on both sides of each word line in the memory cell area and into regions on both sides of each gate electrode in the logic circuit.

2. A method of manufacturing a semiconductor device according to claim 1, wherein:

the logic circuit area of the semiconductor substrate defines therein an n-channel MISFET forming area and a p-channel MISFET forming area;

the impurities doped in said step of doping impurities in the silicon film are n-type impurities, and the region of the silicon film doped with the impurities to have the

second impurity concentration is the n-channel MISFET forming area;

in said step of patterning the silicon film, the gate electrodes having the second impurity concentration are left in the n-channel MISFET area in the logic circuit area and the other gate electrodes made of the silicon film are left in the p-channel MISFET forming area; and

the method further comprising a step of doping p-type impurities into said the other gate electrodes left in the p-channel MISFET forming area and into the substrate surface layer on both sides of each of said the other gate electrodes.

3. A method of manufacturing a semiconductor device according to claim 1, wherein said step of forming source/drain regions comprises:

a first ion implantation step of implanting impurity ions into the substrate surface layer on both sides of each of the gate electrodes in the logic circuit area and in the memory cell area by using the gate electrodes as a mask;

a step of depositing a first insulating film over a whole surface of the semiconductor substrate;

a step of leaving a first side wall insulating film on each side wall of each gate electrode in the logic circuit, by covering an area of the first insulating film in the memory cell area with a resist pattern and anisotropically etching the first insulating film in the logic circuit area;

a second ion implantation step of implanting impurity ions into the substrate surface layer on both sides of each gate electrode in the logic circuit area, by using as a mask the gate electrodes in the logic circuit area and the first side wall insulating film; and

a step of forming a metal silicide film on an upper surface of each gate electrode in the logic circuit and on surfaces of the source/drain regions on both sides of

each gate electrode.

4. A method of manufacturing a semiconductor device according to claim 3, wherein in said first ion implantation step, phosphorous ions are implanted in the memory cell area and at least arsenic ions are implanted in the logic circuit area.

5. A semiconductor device comprising:

a semiconductor substrate having a memory cell area and a logic circuit area defined on a principal surface of the semiconductor substrate;

a plurality of memory cells disposed in the memory cell area of said semiconductor substrate, each memory cell including a first MISFET and a capacitor, and a gate electrode of each first MISFET having a first impurity concentration; and

a plurality of second MISFET's disposed in the logic circuit area of said semiconductor substrate, each second MISFET having a conductivity type same as a conductivity type of the first MISFET and a gate electrode of each second MISFET having a second impurity concentration lower than the first impurity concentration.

6. A semiconductor device according to claim 5, wherein an upper surface of the gate electrode of each second MISFET and upper surfaces of source/drain regions thereof are formed with a metal silicide film, and an upper surface of the gate electrode of each first MISFET and upper surfaces of source/drain regions thereof are not formed with a metal silicide film.

7. A method of manufacturing a semiconductor device comprising the steps of:

preparing a semiconductor substrate having a memory cell area and a logic

circuit area defined on a principal surface of the semiconductor substrate;

forming an element separation structure made of insulating material in a partial area of the principal surface of the semiconductor substrate to define active regions;

forming first gate insulating films in areas of the principal surface of the semiconductor substrate where the element separation structure is not formed;

forming a first conductive film covering the element separation structure and the first gate insulating films;

removing the first conductive film in the memory cell area;

forming a capacitor dielectric film on a surface of the first conductive film;

forming a second conductive film on the capacitor dielectric film and on the semiconductor substrate;

patterning the second conductive film to leave an upper electrode over the element separation structure and to leave a plurality of word lines serving as gate electrodes in the memory cell area; and

patterning the capacitor dielectric film and the first conductive film to leave a lower electrode made of the first conductive film, in which the lower electrode is left in a pattern inclusive of the upper electrode as viewed along a direction normal to the semiconductor substrate, a gate electrode made of the first conductive film is left over the active region in the logic circuit area, and the capacitor dielectric film is left between the upper and lower electrodes.

8. A method of manufacturing a semiconductor device according to claim 7, further comprising a step of removing the first gate insulating film in the memory cell area, after said step of removing the first conductive film in the memory cell area and before said step of forming the capacitor dielectric film, wherein said step of forming the

capacitor dielectric film further comprises a step of forming a second gate insulating film on the principal surface of the semiconductor substrate in the memory cell area.

9. A method of manufacturing a semiconductor device according to claim 7, further comprising:

a step of forming a first side wall insulating film on a side wall of each gate electrode in the logic circuit, and embedding a space between word lines in the memory cell area with an embedding insulating member of insulating material;

a step of implanting impurities into a substrate surface layer on both sides of the gate electrode in the logic circuit area; and

a step of forming a metal silicide film on an upper surface of the gate electrode in the logic circuit area and on a surface of the semiconductor substrate on both side of the gate electrode.

10. A method of manufacturing a semiconductor device according to claim 8, further comprising:

a step of depositing an upper insulating film on the second conductive film after said step of forming the second conductive film, the upper insulating film made of insulating material having an etching resistance different from the embedding insulating member, wherein in said step of patterning the second conductive film, the upper insulating film is patterned to have a same pattern as the second conductive film; and

a step of forming a second side wall insulating film on a side wall of each word line after said step of leaving the word lines, the second side wall insulating film being made of insulating material having an etching resistance different from the embedding insulating member, wherein the embedding insulating member is filled in between the second side wall insulating films disposed on opposing side walls of adjacent

word lines.

11. A semiconductor device comprising:

a semiconductor substrate having a memory cell area and a logic circuit area defined on a principal surface of the semiconductor substrate, and element separation structures formed on surfaces of the logic circuit area and the memory cell area;

a plurality of memory cells disposed on said semiconductor substrate in the memory cell area, each memory cell including a first MISFET and a capacitor and a gate electrode of the first MISFET having a first structure;

a plurality of second MISFET's disposed on said semiconductor surface in the logic circuit area, each second MISFET having a same conductivity type as a conductivity type of the first MISFET and a gate of each second MISFET having a second structure; and

a capacitor disposed on the element separation structure in the logic circuit area, the capacitor having a lower electrode, a capacitor dielectric film, and an upper electrode stacked in this order, wherein the upper electrode has the first structure and the lower electrode has the second structure.

12. A semiconductor device comprising:

MISFET's formed on a surface of a semiconductor substrate, each MISFET including source/drain regions and a gate electrode disposed above a channel region between the source/drain regions;

a cover insulating film made of insulating material and covering an upper and side wall of the gate electrode;

a conductive pad disposed covering a corresponding upper surface of the

source/drain regions and corresponding side wall of said cover insulating films;

an interlayer insulating film disposed over the semiconductor substrate and covering said pad and said MISFET's;

a contact hole formed in said interlayer insulating film at a position included by said pad as viewed along a direction normal to the semiconductor substrate; and

a capacitor formed on said interlayer insulating film, one electrode of said capacitor being connected via said contact hole to said pad.

13. A method of manufacturing a semiconductor device comprising the steps of:

preparing a semiconductor substrate having a memory cell area and a logic circuit area defined on a principal surface of the semiconductor substrate;

forming a DRAM circuit on the semiconductor substrate in the memory cell area, wherein the DRAM circuit includes a plurality of memory cells and bit lines, each memory cell has a pair of MISFET and capacitor, one electrode of the capacitor is connected to one region of source/drain regions of a corresponding MISFET, the bit line interconnects the other regions of source/drain regions of MISFET's of some memory cells, the bit line extends near to a boarder line between the memory cell area and the logic circuit area, the other opposing electrode of the capacitor is disposed on a layer higher than the bit line and connected to a plurality of capacitors, a first insulating film electrically insulates the bit lines and MISFET's, a second insulating film electrically insulates the bit lines and capacitors, and the opposing electrode and first and second insulating films are also disposed in the logic circuit area;

covering a surface of the opposing electrode in the memory cell area with a resist pattern, wherein a boarder of the resist pattern is positioned apart from a front end

of the bit lines toward the logic circuit area;

isotropically etching the opposing electrode to remove the opposing electrode in the logic circuit area, by using the resist pattern as a mask, wherein the opposing electrode in the logic circuit area is also side-etched until a border of the opposing electrode retracts from the front end of the bit line;

etching and removing the first and second interlayer insulating films in the logic circuit area by using the resist pattern as a mask;

covering a whole surface of the semiconductor substrate with a third interlayer insulating film;

forming a contact hole in the third and second interlayer insulating films, the contact hole being formed at a position away from the boarder of the opposing electrode toward the logic circuit area and exposing a partial upper surface of the bit line; and

forming a wiring on the third insulating film, the wiring being connected via the contact hole to the bit line and extending in the logic circuit area.

14. A semiconductor device comprising:

a semiconductor substrate having a memory cell area and a logic circuit area defined on a principal surface of the semiconductor substrate;

an element separation structure formed on said semiconductor substrate in a boarder area between the memory cell area and the logic circuit area;

an interconnect wiring disposed on said element separation structure;

a DRAM circuit formed on the semiconductor substrate in the memory cell area, wherein the DRAM circuit includes a plurality of memory cells and bit lines, each memory cell has a pair of MISFET and capacitor, one electrode of the capacitor is connected to one region of source/drain regions of a corresponding MISFET, the bit line

interconnects the other regions of source/drain regions of MISFET's of some memory cells, the bit line extends near to a boarder line between the memory cell area and the logic circuit area, and the bit line is disposed on a layer higher than the interconnect wiring and connected thereto;

an interlayer insulating film covering said DRAM circuit and the logic circuit area;

a contact hole formed through said interlayer insulating film, a bottom of said contact hole being a partial upper surface of said interconnect wiring; and

an upper wiring disposed on said interlayer insulating film, said upper wiring being connected via said contact hole to said interconnect wiring and extending in the logic circuit area.

15. A method of manufacturing a semiconductor device comprising the steps of:

preparing a semiconductor substrate having a memory cell area and a logic circuit area defined on a principal surface of the semiconductor substrate;

forming a gate insulating film on the principal surface of the semiconductor substrate;

forming a silicon film on the gate insulating film;

doping impurities into the silicon film to make a region of the silicon film in the memory cell area having a first impurity concentration;

patterning the silicon film to leave word lines having the first impurity concentration and serving as gate electrodes in the memory cell area and to leave gate electrodes in the logic circuit area;

forming source/drain regions of MISFET's in a surface layer of the semiconductor substrate by doping impurities into regions on both sides of each word line

in the memory cell area; and

forming source/drain regions of MISFET's in a surface layer in the logic circuit area of the semiconductor substrate and doping impurities into the gate electrode in the logic circuit area at the same time so that the gate electrodes in the logic circuit area have second impurity concentration lower than the first impurity concentration.